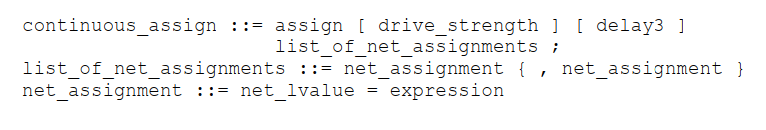
Prob 2:

1. **Statement assign**

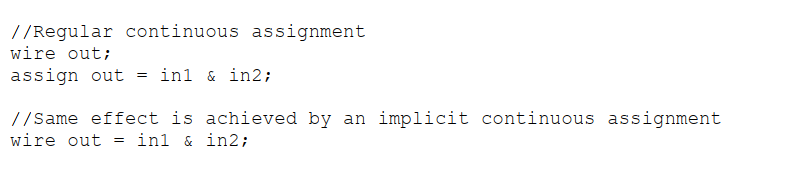
A continuous assignment is the most basic statement in dataflow modelling, used to drive a value onto a net. This assignment replaces gates in the description of the circuit and describes the circuit at a higher level of abstraction. The assignment statement starts with the keyword assign



Some further notations for the assignment:

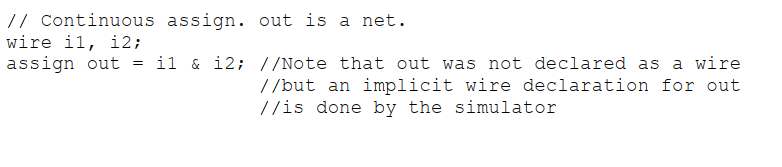
* The left hand side of an assignment must always be a scalar or vector net or a concatenation of scalar and vector nets. It cannot be a scalar or vector register
* Continuous assignments are always active. The assignment expression is evaluated as soon as one of the right-hand-side operands changes and the value is assigned to the left hand side net
* The operands on the right-hand side can be registers or nets or function calls. Registers or nets can be scalars or vectors.
* Delay values can be specified for assignments in terms of time units. Delay value are used to control the time when a net is assigned the evaluated value. This feature is similar to specifying delays for gates. It is very useful in modeling timing behavior in real circuits.
  1. Implicit Continuous Assignment

Instead of declaring a net and then writing a continuous assignment on the net, Verilog provides a shortcut by which a continuous assignment can be placed on a net when it is declared. There can be only 1 implicit declaration assignment per net because a net is declared only once.



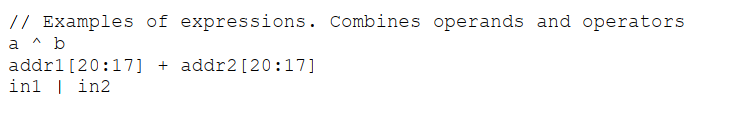
* 1. Implicit Net Declaration

If a signal name is used to the left of the continuous assignment, an implicit net declaration will be inferred for that signal name. If the net is connected to a modul port the width of the inferred net is equal to the width of the module port



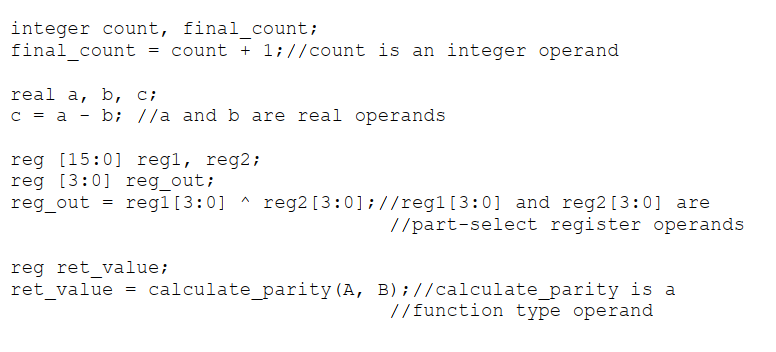
1. **Define, examples of expressions, operands, operator in Dataflow Modelling**
   1. Expressions

* Are constructs that combine operators and operands to produce a result



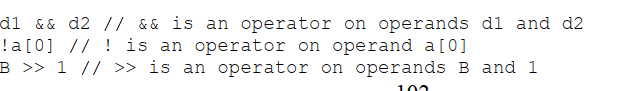
* 1. Operands

There are varied data types. Some constructs will take only certain types of operands. Operands can be constants, integers, real numbers, nets, registers, times, bit select, part select, memories or function calls



* 1. Operators

Act on the operands to produce desired results as various types of operators are provided in Verilog



1. **Dataflow Modelling operators**

This provides many different operator types. Operators can be arithmetic, logical, relational, equality, bitwise, reduction, shift, concatenation or conditional.

